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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,044	08/25/2000	CHANDRA V. MOULI	MIO 0054 PA	6800

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/05/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

P-5

Office Action Summary

Application No.	Applicant(s)
09/648,044	Mouli et al.
Examiner	**Art Unit**
ORI NADAV	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Nov 9, 2001*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above, claim(s) *15-44* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Aug 25, 2000* is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicant's election of claims 1-14 in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a gate electrode comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks), a gate electrode comprised of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer, and a CMOS device having all the claimed limitations as recited in claims 12 and 14, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Specification

3. The abstract of the disclosure is objected to because the abstract recites a method of making a device, whereas the claims are directed to a device. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities: On page 8, line 4, the term "if" should read "of".

Appropriate correction is required.

Claim Objections

5. Claims 3 and 10 are objected to because of the following informalities: Claim 3 recites the limitation "the portion" in line 7. There is insufficient antecedent basis for this limitation in the claim. Claim 10 recites the limitation "the titanium layer" in line 3. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (5,750,435).

Pan teaches in figure 1e a circuit structure comprising a semiconductor layer 10; a source region and a drain region 24 in the semiconductor layer which are lightly doped and heavily doped with a first conductivity-type dopant; a channel region located between the source/drain regions; a gate oxide layer 14 located on a surface of the channel region; and a gate electrode 16 (column 5, lines 39-42) comprising polysilicon and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks) having a defined leading edge located on the gate oxide layer, the portion of the gate oxide layer which is beneath the gate electrode and adjacent the leading edge and adjacent the drain region, and which defines an overlap region, having an ion implant concentration comprising fluorine which is effective to lower the surface electrical field in the overlap region (column 6, lines 37-44), and including a pair of spaces adjacent the gate electrode.

Although Pan does not explicitly state that the fluorine is effective to lower the surface electrical field in the overlap region, the fluorine is effective to lower the surface electrical field in the overlap region. Therefore, the claimed structure is considered to be at least obvious over Pan's structure.

Regarding claims 2, 4 and 13, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a fluorine concentration of about 1 E 18 atoms per cubic centimeter in Pan's device, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 11, Pan teaches in figure 1e a pair of conductive studs 28 and an interlevel dielectric layer 26 provided on the semiconductive layer, the interlevel dielectric layer have a pair of through bores, each accommodating one of each the pair of conductive studs, and one of each the pair of conductive studs contacting one of each the source/drain regions.

Regarding claims 12-14, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Pan's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (5,750,435) in view of Admitted Prior Art (APA).

Pan teaches substantially the entire claimed structure, as applied to claim 1 above, except a gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium

layer. APA teaches in figure 1 a gate electrode is comprised of a layer of polysilicon 18, a layer of titanium nitride 20 deposited on the polysilicon layer, and a layer of tungsten 22 deposited on the titanium layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate electrode comprising of a layer of polysilicon, a layer of titanium nitride deposited on the polysilicon layer, and a layer of tungsten deposited on the titanium layer in Pan's device, in order to reduce the contact resistance of the device.

9. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (5,750,435) in view of Motoyoshi et al. (JP 6-53492).

Pan teaches substantially the entire claimed structure, as applied to claim 1 above, except using the transistor in a CMOS configuration.

Motoyoshi et al. use a transistor having a gate oxide comprising fluorine in a CMOS configuration. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Pan's transistor in a CMOS configuration in order to use the device in a specific application which requires a CMOS device.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

November 19, 2001

Steven Loke
Primary Examiner